REMARKS

The Office Action mailed August 25, 2004 has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

Information Disclosure Statement

Acknowledgement of the Information Disclosure Statement filed on January 12, 2004, whose receipt was acknowledged in a telephone inquiry to the Examiner on November 22, 2004, is respectfully requested.

Specification/Title of the Invention

The Title of the Invention has been changed in order to be more descriptive.

Subject Matter Indicated Allowed or Allowable

Applicants gratefully acknowledge the indication of allowability of Claim 38, subject to its re-writing in independent form. For the reasons outlined below, it is believed that base claim 36 is allowable in its own right, and re-writing Claim 38 to include the limitations of Claim 38 is therefore unnecessary.

Rejection(s) Under 35 U.S.C. § 103 Rejection

Claims 36 – 37 and 39 – 40 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Diorio et al. (U.S. pat. no. 5,990,512) in view of Alavi et al. (U.S. pat. no. 5,844,300). The Office Action contends that it would have been obvious to include p+ doped third and fourth regions of Alavi et al. in the second n-well of Diorio et al. because these two

patents "are from the same field of endeavor (pFET transistors)," and "the purpose disclosed in Alavi et al. would have been recognized in the pertinent art of Diorio et al." Therefore, it is alleged, "it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the pFET synapse transistor structure as taught by Diorio et al. with the structure having third and fourth p+ doped regions disposed in a second well as taught by Alavi et al. to develop a structure capable of monitoring electrostatic charge." Applicants respectfully disagree.

First, it will be noted that Diorio et al. is directed to a device for storing charge as part of its operation, as most clearly seen from the title ("...Mechanism for Long Term Learning"). In contradistinction, Alavi et al. is directed to a device for monitoring charge buildup during fabrication. Thus, while both Diorio et al. and Alavi et al. contain pFETs, it cannot be contended that such incidental overlap is sufficient to provide motivation to combine their teachings. The Examiner's own reasoning, that "it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the pFET synapse transistor structure as taught by Diorio et al. with the structure having third and fourth p+ doped regions disposed in a second well as taught by Alavi et al. *to develop a structure capable of monitoring electrostatic charge*" bears this out simply because Diorio et al. is NOT concerned with monitoring electrostatic charge, and therefore the ordinarily skilled artisan working in the different field of memory and learning of Diorio et al. would not look for guidance to the teachings Alavi et al., which is in the field of monitoring electrostatic charge.

Second, it will be appreciated that the mere disclosure in Alavi et al. of third and fourth p+ doped regions disposed in a second n-well in one device is no guarantee that such features can

also be provided and be operable in the second, different device of Diorio et al.. Numerous other factors must be taken into account, rendering such a modification far from obvious. For instance, higher differential voltages may be imposed, erecting higher tunneling and injection barriers, and removing the device from a useful operating range. This is particularly apparent because the structure of the Alavi et al. device is at its core an EEPROM, and includes a central transistor 48 having no counterpart in Diorio et al.

Finally, the presently claimed invention seeks as one of its objectives to provide devices that are simple to fabricate, in accordance with standard CMOS production procedures. Consistent with such procedures is the use of a single layer polycrystalline silicon floating gate. Newly added Claims 44 and 46 are specifically directed to such a device, with Claim 44 stating that the inventive synapse transistor "is configured to operate as a current source without gate input using a single polysilicon gate layer," and Claim 46 reciting "a single polysilicon layer disposed above [the] layer of gate oxide, said single polysilicon layer comprising a floating gate." Support for these feature can be found in the specification at, for example, page 10, lines 9 – 13. Newly added Claim 45 and 47 are also consistent with this objective, with Claim 45 reciting a pFET synapse transistor which is part of "[a] system on a chip (SOC) including digital and analog circuits integrated on a single semiconductor chip." (See page 3, paragraph 0003 of the specification for support). Newly added Claims 48 – 52 are directed to a novel p-channel floating gate device which is patentable over the applied prior art for at least the same reasons set forth above.

Conclusion

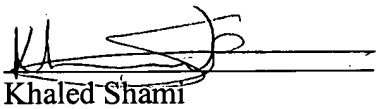
In view of the preceding discussion, Applicants respectfully urge that the claims of the present application define patentable subject matter and should be passed to allowance. Such allowance is respectfully solicited.

If the Examiner believes that a telephone call would help advance prosecution of the present invention, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Reply, or credit any overpayment not otherwise paid or credited, to our deposit account No. 50-1698.

Respectfully submitted,
THELEN REID & PRIEST, L.L.P.

Dated: November 24, 2004



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